

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

1. Introduction

This application note serves as a guide to compare the Micron N25Q032A and N25Q064A with the Macronix MX25U3235F and MX25U6435F 1.8V 32Mb and 64Mb Serial Flash. The document does not provide detailed information on each individual device, but highlights the similarities and differences between them. The comparison covers the general features, performance, command codes, and other differences.

If common features are used in standard traditional modes, they may need only minimal software modification.

The information provided in this document is based on datasheets listed in Section 9. Newer versions of the datasheets may override the contents of this document.

2. Features

Both flash device families have similar features and functions as shown in Table 2-1.

Table 2-1: Feature Comparison

Feature	Macronix MX25U_35F	Micron N25Q_A
VCC Voltage Range	1.65V-2.0V	1.7V-2.0V
Normal Read Clock Frequency	50MHz ⁽¹⁾	54MHz
Fast Read (1-1-1)	Yes	Yes
Dual Output (DREAD) (1-1-2)	-	Yes
Dual I/O (2READ) (1-2-2)	Yes	Yes
Dual Peripheral Interface (2-2-2)	-	Yes
Quad Output (QREAD) (1-1-4)	-	Yes
Quad I/O (4READ) (1-4-4)	Yes	Yes
Quad Peripheral Interface (QPI) (4-4-4)	Yes	Yes
XIP / Performance Enhanced Mode	Yes	Yes
Sector Size	4KB/32KB/64KB	4KB/64KB
Program Buffer Size	256Byte	256Byte
Security OTP	512Byte	64Byte
Program/Erase Suspend & Resume	Yes	Yes
Wrap Around Burst Read Mode	Yes	Yes
Configurable Dummy Cycle	Yes	Yes
Adjustable Output Driver	-	Yes
Deep Power Down	Yes	Yes
S/W Reset Command	Yes	Yes
HOLD#/RESET# Pin	Reset#	Hold#/Reset#
Block Protection Mode (BP bits)	Yes	Yes
Individual Sector Protection Mode (Volatile)	Yes	Yes
Program/Erase Cycles	100K	100K

Notes: 1) The maximum clock rate=33MHz when reading secured OTP area.

**Comparing Micron N25Q032A / N25Q064A
with Macronix MX25U3235F / MX25U6435F**

Table 2-2: Read Performance

I/O Mode	Macronix MX25_35F		Micron N25Q_A	
	Default Dummy Cycles	Max Speed @ Default Dummy Cycles	Default Dummy Cycles	Max Speed @ Default Dummy Cycles
Fast Read (1-1-1)	8	104MHz	8	108MHz
Dual Output (DREAD) (1-1-2)	-	-	8	108MHz
Dual I/O (2READ) (1-2-2)	4	84MHz	8	108MHz
Dual Peripheral Interface (2-2-2)	-	-	9	108MHz
Quad Output (QREAD) (1-1-4)	-	-	8	108MHz
Quad I/O (4READ) (1-4-4)	6	104MHz	10	108MHz
Quad Peripheral Interface (QPI) (4-4-4)	6	104MHz	11	108MHz

**Comparing Micron N25Q032A / N25Q064A
with Macronix MX25U3235F / MX25U6435F**

3. Package and Pinout

Both devices are available in 8-pin SOP and 8-WSON packages with similar footprints. Pinout definitions are identical with the two exceptions shown in Table 3-2. Where Macronix has a RESET#/SIO3 pin, Micron has either a HOLD#/DQ3 or a RESET#/DQ3 pin. If the Micron device has a RESET# pin, then the devices are pin compatible. If the Micron device has a HOLD# pin, but the HOLD# function is not used, then the devices are also pin compatible. Macronix does not support the VPP (10V Fast Programming Voltage) function available on Micron's W#/VPP/DQ2 pin. This function is normally only used on external programmers to accelerate Program/Erase operations and is generally not used for "in-circuit" programming. Please consult the latest Macronix datasheet for any possible package additions.

Table 3-1: Packages

Packages	MX25U_35F	N25Q_A
8-WSON (6x5mm)	YES	YES
8-WSON (8x6mm)	-	YES
8-SOP (209mil)	YES	YES
16-SOP (300mil)	-	YES
24-TFBGA	-	YES

Table 3-2: Pin Definition Comparison

Pin Number	Macronix MX25U_35F	Micron N25Q_A	Comments
Pin #1	CS#	S#	-
Pin #2	SO/SIO1	DQ1	-
Pin #3	WP#/SIO2	W#/ V _{PP} /DQ2	Macronix does not support V _{PP}
Pin #4	GND	VSS	-
Pin #5	SI/SIO0	DQ0	-
Pin #6	SCLK	C	-
Pin #7	RESET#/SIO3	HOLD#/DQ3 or RESET#/SIO3	HOLD# not supported by Macronix. Dedicated Micron part numbers offer RESET# instead of HOLD#.
Pin #8	VCC	VCC	-

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

4. Key Feature and Operational Differences

4-1 Status Register and Configuration Register Differences

Both devices use registers to control device behavior and report status. The registers and bits used are similar but not identical. Both the Micron and Macronix devices use BP bits to select groups of memory areas for protection.

The N25Q032/64A Block Protection bits BP[2:0] are located in Status Register (bits [4:2]). The Top/Bottom bit is located in Status Register bit 5 and selects whether block protection starts at the top or bottom of memory. The BP[2:0] and Top/Bottom bits are nonvolatile and reprogrammable.

The MX25U32/6435F Block Protection bits BP[3:0] are located in Status Register bits [5:2]. The block protection starts at the top of memory, and the protected upper areas are the same. The BP[3:0] bits are all nonvolatile and reprogrammable. The granularity of Write protection is different between the Macronix and Micron devices if block protection starts at the bottom of memory, but the same if protection starts at the top of memory.

4-2 QPI Differences

Micron's Quad I/O mode is entered by setting a bit in the Nonvolatile Configuration Register (NVCR), which remembers this mode after power cycles, or by setting a bit in the Enhanced Volatile Configuration Register (VCR) and is reset after a power cycle.

The MX25U32/6435F requires an EQIO (35h) command to enter the equivalent QPI mode. This mode can be terminated by a RSTQIO (F5h) command or by a power cycle or software reset.

4-3 XIP Differences

The XIP (eXecute In Place) feature (Macronix refers to this as Performance Enhance Mode) is only used during Fast Read operations and eliminates the need to input read commands prior to entering an address and reading data. This is an overhead reduction feature that increases data throughput. Both devices offer this feature, but entry and exit methods are different.

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

4-4 Individual Sector Protection Differences

Both devices have the ability to write protect individual 64KB sectors/blocks of memory. Individual Sector Protection does not use the nonvolatile BP bits in the Status Register. With the Micron flash, it is possible to use both methods of write protection (BP bits and Individual Sector Protection) simultaneously, and the protected area is the combination of the two. When using the Macronix flash, either BP bit Protection or Individual Sector Protection can be selected exclusively, with the default being the use of the BP bits.

The N25Q_A have one volatile Lock Register for each 64KB sector to control the sector's program/erase protection status. The protection can be turned on or off at any time unless the sector's Lock Register has been locked by the application. Once locked, its associated sector will remain in the protected or unprotected state until the next power cycle or reset. All sectors not protected by the Status Register BP configuration will be unprotected after power up and all Lock Registers will be unlocked.

The MX25U_35F have one volatile protection register for each of the top sixteen 4KB sectors, bottom sixteen 4KB sectors, and the remaining middle 64KB blocks (the MX25U3235F has 62 middle blocks and the MX25U6435F has 126 middle blocks). These protection registers can only be used after permanently disabling the Status Register BP protection bits. This is done by executing the WPSEL instruction once. Please note that this irreversible and Individual Sector Protection method will be permanently selected.

After permanently selecting the Individual Sector Protection method for the MX25U_35F, all sectors and blocks will be locked by default on power up. Sectors/blocks must be unlocked before they can be programmed or erased. Unlocking sectors/blocks can be done on an individual basis with the SBULK (Single Block Unlock) command or on all sectors/blocks with the GBULK (Global Block Unlock) command. Sectors and blocks can be relocked as necessary with the SBLK (Single Block Lock) command or GBLK (Global Block Lock) command.

Since the smallest individual sector protection size in the N25Q_A is 64KB, if an application is currently locking/unlocking the top and/or bottom 64KB sector(s), it will need to lock/unlock each of the 16 top and/or bottom 4KB sectors in the MX25U_35F for equivalent results.

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

5. Performance

Table 5-1 and 5-2 show that the two devices have similar AC and DC performance.

Table 5-1: AC Parameter Comparison

Parameter	Symbol		Condition	Macronix MX25U_35F	Micron N25Q_A
	Macronix	Micron			
Clock High / Low Time	tCH / tCL	tCH / tCL	min	4.5ns	4ns
Clock Low to Output Valid	tCLQV	tCLQV	max @10pF	-	5ns
			max @15pF	6ns	-
			max @30pF	8ns	7ns
Data In Setup Time	tDVCH	tDVCH	min	2ns	2ns
Data In Hold Time	tCHDX	tCHDX	min	3ns	3ns
Page Program Time (256 Bytes)	tPP	tPP	typ	1.2ms	0.5ms
			max	3ms	5ms
Erase 4KB Subsector/Sector	tSSE	tSE	typ	60ms	250ms
			max	200ms	800ms
Erase 32KB Sector	tBE32	-	typ	250ms	-
			max	1s	-
Erase 64KB Sector/Block	tBE	tSE	typ	500ms	700ms
			max	2s	3s
Bulk Erase / Chip Erase (32Mb)	tCE	tBE	typ	25s	30s
			max	50s	60s
Bulk Erase / Chip Erase (64Mb)	tCE	tBE	typ	50s	60s
			max	100s	120s

Table 5-2: DC Parameter Comparison

Parameter	Symbol		Condition	Macronix MX25U_35F	Micron N25Q_A
	Macronix	Micron			
Leakage Current	ILI/ILO	ILI/ILO	max	+/- 2uA	+/- 2uA
Standby Current	ISB1	ICC1	max	80uA	100uA
Deep Power Down Current	ISB2	ICC2	typ	5uA	-
			max	20uA	10uA
VCC Read Current (Fast Read)	ICC1	ICC3	max @108MHz (Quad I/O)	-	20mA
			max @104MHz (Quad I/O)	20mA	-
			max @ 84MHz	15mA	-
			max @ 54MHz	-	6mA
VCC Program Current	ICC2	ICC4	max	25mA	20mA
VCC Write Status Register Current	ICC3	ICC5	max	20mA	20mA
VCC Erase Current	ICC4,5	ICC6	max	25mA	20mA

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

6. Command Code

Both devices use the same basic command set, but there are a few minor differences highlighted in Table 6-1.

Table 6-1: Command Code Comparison

Instruction Type	Instruction	Description	Macronix MX25U3_35F	Micron N25Q_A
Read ID	RDID	Read Identification	9Fh	9Eh/9Fh
	REMS	Read Electronic Manufacturer ID &	90h	-
Read	READ	Read Data Bytes	03h	03h
	FAST_READ	Read Data Bytes at Higher Speed	0Bh	0Bh
	DOFR	Dual Output Fast Read	-	3Bh
	DIOFR	Dual Input/Output Fast Read	BBh	BBh
	QOFR	Quad Output Fast Read	-	6Bh
	QIOFR	Quad Input/Output Fast Read	EBh	EBh
	W4READ	Quad Input/Output Fast Read	E7h	-
	RDSFDP	Read Serial Flash Discoverable Parameters	5Ah	5Ah
Write	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
	PP	Page Program	02h	02h
	-	Dual Input Fast Program (1-1-2)	-	A2h
	-	Dual I/O Fast Program (1-2-2)	-	D2h
	-	Quad Input Fast Program (1-1-4)	-	32h
	4PP	Quad Page Program (1-4-4)	38h	12h
	SE	Sector Erase 4KB	20h	20h
	BE 32K	Block Erase 32KB	52h	-
	SE 64K	Block Erase 64KB	D8h	D8h
	CE	Chip Erase	60 or C7h	C7h
OTP	ENSO	Enter Secured OTP	B1h	-
	EXSO	Exit Secured OTP	C1h	-
	ROTP	Read OTP Area	-	4Bh
	POTP	Program OTP Area	-	42h
QPI	EQIO	Enable QPI	35h	-
	RSTQIO	Reset (Exit) QPI	F5h	-
	QPIID	QPI ID Read	AFh	AFh

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

Table 6-1: Command Code Comparison - Continued

Instruction Type	Instruction	Description	Macronix MX25U_35F	Micron N25Q_A
Registers	RDSR	Read Status Register	05h	05h
	WRSR	Write Status Register	01h	01h
	RDSCUR	Read Security Register	2Bh	-
	WRSCUR	Write Security Register	2Fh	-
	RDLR	Read Lock Register	-	E8h
	WRLR	Write Lock Register	-	E5h
	RFSR	Read Flag Status Register	-	70h
	CLFSR	Clear Flag Status Register	-	50h
	-	Read Non-volatile Configuration Register	-	B5h
	-	Write Non-volatile Configuration Register	-	B1h
	-	Read Volatile Configuration Register	-	85h
	-	Write Volatile Configuration Register	-	81h
	-	Read Enhance Volatile Configuration Register	-	65h
	-	Write Enhance Volatile Configuration Register	-	61h
	PGM/ERS Suspend	Program or Erase Suspend	B0h	75h
	PGM/ERS Resume	Program or Erase Resume	30h	7Ah
	RSTEN	Reset Enable	66h	66h
	RST	Reset Memory	99h	99h
	SBL	Set Burst Length	C0h	Note 1
	NOP	No Operation	00h	-
	DP	Deep Power Down	B9h	B9h
	RDP	Release From Deep Power Down	ABh	ABh
	WPSEL	Write Protect Selection (OTP)	68h	-
	GBLK	Gang Block Lock	7Eh	-
	GBULK	Gang Block Unlock	98h	-
	SBLK	Single Block Lock	36h	-
	SBULK	Single Block UnLock	39h	-
	RDBLOCK	Read Block Lock	3Ch	-

Note 1: Micron uses a Volatile Configuration Register to control this function.

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

7. Manufacturer and Device ID

Table 7-1: Manufacturer and Device ID Comparison

ID Type	Macronix		Micron	
	MX25U3235F	MX25U6435F	N25Q32A	N25Q64A
Manufacturer ID	C2h	C2h	20h	20h
JEDEC ID	2536h	2537h	BB16h	BB17h
Unique ID	N/A	N/A	17 Bytes	17 Bytes

8. Summary

The Macronix MX25U3235F/6435F and Micron N25Q032/64A have similar commands, functions, and features. The devices are command compatible for basic read, program, and erase (4KB and 64KB) operations. The devices are essentially pin compatible if the HOLD# function is not used. A more detailed analysis should be done if “special” functions such as XIP, Suspend/Resume, or Accelerated Programming are used. If common features are used in standard traditional modes, they may need only minimal software modification.

9. References

Table 9-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed Macronix specification, please refer to the Macronix Website at <http://www.macronix.com/>.

Table 9-1: Datasheet Version

Datasheet	Location	Date Issued	Version
MX25U3235F	Macronix Website	FEB. 3, 2012	1.0
MX25U6435F	Macronix Website	FEB. 3, 2012	1.0
n25q_32mb_1_8v_65nm	Micron Website	APR. 2013	G
n25q_64mb_1_8v_65nm	Micron Website	APR. 2013	G

Comparing Micron N25Q032A / N25Q064A with Macronix MX25U3235F / MX25U6435F

10. Appendix

Table 10-1 shows the basic part number and package information cross reference between Macronix MX25U3235F and Micron N25Q032A parts.

Table 10-2 shows the basic part number and package information cross reference between Macronix MX25U6435F and Micron N25Q064A parts.

Table 10-1: 32Mb Part Number Cross Reference

Macronix Part No.	Micron Part No.	Package	Dimension	Note
MX25U3235FM2I-10G	N25Q032A11ESE40	8-SOP	209 mil	Hold# pin, Micron XIP
MX25U3235FM2I-10G	N25Q032A21ESE40	8-SOP	209 mil	Hold# pin, basic XIP
MX25U3235FM2I-10G	N25Q032A31ESE40	8-SOP	209 mil	Reset# pin, Micron XIP
MX25U3235FM2I-10G	N25Q032A41ESE40	8-SOP	209 mil	Reset# pin, basic XIP
MX25U3235FZNI-10G	N25Q032A11EF640	8-WSON	6x5 mm	Hold# pin, Micron XIP
MX25U3235FZNI-10G	N25Q032A21EF640	8-WSON	6x5 mm	Hold# pin, basic XIP
MX25U3235FZNI-10G	N25Q032A31EF640	8-WSON	6x5 mm	Reset# pin, Micron XIP
MX25U3235FZNI-10G	N25Q032A41EF640	8-WSON	6x5 mm	Reset# pin, basic XIP

Table 10-2: 64Mb Part Number Cross Reference

Macronix Part No.	Micron Part No.	Package	Dimension	Note
MX25U6435FM2I-10G	N25Q064A11ESE40	8-SOP	209 mil	Hold# pin, Micron XIP
MX25U6435FM2I-10G	N25Q064A21ESE40	8-SOP	209 mil	Hold# pin, basic XIP
MX25U6435FM2I-10G	N25Q064A31ESE40	8-SOP	209 mil	Reset# pin, Micron XIP
MX25U6435FM2I-10G	N25Q064A41ESE40	8-SOP	209 mil	Reset# pin, basic XIP
MX25U6435FZNI-10G	N25Q064A11EF640	8-WSON	6x5 mm	Hold# pin, Micron XIP
MX25U6435FZNI-10G	N25Q064A21EF640	8-WSON	6x5 mm	Hold# pin, basic XIP
MX25U6435FZNI-10G	N25Q064A31EF640	8-WSON	6x5 mm	Reset# pin, Micron XIP
MX25U6435FZNI-10G	N25Q064A41EF640	8-WSON	6x5 mm	Reset# pin, basic XIP

11. Revision History

Revision	Description	Date
1.0	Initial Release	June 4, 2013



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APPLICATION NOTE

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