

Migrating from MX30UF4G28AB to MX30UF4G28AC

1. Introduction

This application note is a guide for migrating Macronix NAND device from the MX30UF4G28AB to the MX30UF4G28AC. The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information in this document is based on datasheets listed in Section 8. Newer versions of the datasheets may override the contents of this document.

2. General Features

Except for the different settings of the “block protection” feature, the extended spare are size (from 112B to 128B per page) of the MX30UF4G28AC, and the 48-TSOP which is not offered by MX30UF4G28AC; both flash devices have similar features and functions as shown in **Table 2-1**. Feature differences are highlighted in ***Bold Italic*** type in the table.

Table 2-1. Key Features Comparison

Part Name	MX30UF4G28AB	MX30UF4G28AC
Voltage	1.7V-1.95V	1.7V-1.95V
Bus Width	x8	x8
Operating Temperature	-40°C to 85°C	-40°C to 85°C
Interface	ONFI 1.0 Compliant	ONFI 1.0 Compliant
Page Size	(2K+112)B	(<i>2K+128</i>)B
Block Size	(128K+7K)B	(<i>128K+8K</i>)B
ECC Requirement	8bit/540B	8bit/ <i>544</i> B
Cache Read/ Cache Program	ONFI Standard	ONFI Standard
OTP	30 Pages	30 Pages
Unique ID	ONFI Standard	ONFI Standard
Block Protection	Setting by boundary address	<i>Setting by BP Bits^{note}</i>
Guaranteed Good Blocks at Shipping	Block#0	Block#0
Data Retention	10 Years	10 Years
Endurance	100K Cycles	100K Cycles
Package	48TSOP (12x20mm) 63-VFBGA (9x11mm)	-- 63-VFBGA (9x11mm)

Note: The Block protection operation is different between these two devices. Please refer to the individual datasheet for detailed specification.

3. Electrical Performance

The key performance specifications are identical for the two devices. **Table 3-1.**

Table 3-1. Key Performance Comparison

Part Name		MX30UF4G28AB			MX30UF4G28AC		
Performance		Min.	Typ.	Max.	Min.	Typ.	Max.
Access Time	Random (tR)	-	-	25us	-	-	25us
	Cache Read	-	5us	25us	-	5us	25us
	Busy time	-	-	-	-	-	-
Program Time	Sequential	25ns	-	-	25ns	-	-
	Page Program	-	320us	600us	-	320us	600us
	Cache Program	-	5us	600us	-	5us	600us
Erase Time	Block	-	1ms	3.5ms	-	1ms	3.5ms
	Standby (TTL)	-	-	1mA	-	-	1mA
	Standby (CMOS)	-	10uA	50uA	-	10uA	50uA
Current Consumption	Active Read	-	23mA	30mA	-	23mA	30mA
	Active Program	-	23mA	30mA	-	23mA	30mA
	Active Erase	-	15mA	30mA	-	15mA	30mA
	Input Leakage	-	-	+/- 10uA	-	-	+/- 10uA
	Output Leakage	-	-	+/- 10uA	-	-	+/- 10uA
Partial-Page Programs	NOP	-	-	4 cycles	-	-	4 cycles

4. Command Set

Except the command sets related to the block protection operation and the two-plane operation in traditional type, other command sets are the same for the two devices (**Table 4-1**).

Table 4-1. Command Set

Part Name	MX30UF4G28AB		MX30UF4G28AC	
	1st Command Cycle	2nd Command Cycle	1st Command Cycle	2nd Command Cycle
Read	00h	30h	00h	30h
Random Data Input	85h	-	85h	-
Random Read Data Output	05h	E0h	05h	E0h
Cache Read Random	00h	31h	00h	31h
Cache Read Sequential	31h	-	31h	-
Cache Read End	3Fh	-	3Fh	-
Read ID	90h	-	90h	-
Parameter Page Read (ONFI)	ECh	-	ECh	-
Read Unique ID (ONFI)	EDh	-	EDh	-
Get Features (ONFI)	EEh	-	EEh	-
Set Features (ONFI)	EFh	-	EFh	-
Reset	FFh	-	FFh	-
Page Program	80h	10h	80h	10h
Cache Program	80h	15h	80h	15h
Block Erase	60h	D0h	60h	D0h
Block Un-Protect Lower^{note}	23h	-	-	-
Block Un-Protect Upper^{note}	24h	-	-	-
Block Protect^{note}	2Ah	-	-	-
Block Solid-Protect^{note}	2Ch	-	-	-
Status Read	70h	-	70h	-
Status Enhanced Read (ONFI)	78h	-	78h	-
Block Protection Status Read	7Ah	-	7Ah	-
Two-plane Program (ONFI)	80h-11h-80h-10h		80h-11h-80h-10h	
Two-plane Cache Program (ONFI)	80h-11h-80h-15h		80h-11h-80h-15h	
Two-plane Block Erase (ONFI)	60h-D1h-60h-D0h		60h-D1h-60h-D0h	
Two-plane Program (Traditional)	--		80h-11h-81h-10h	
Two-plane Cache Program (Traditional)	--		80h-11h-81h-15h	
Two-plane Block Erase (Traditional)	--		60h-60h-D0h	

Note: These command sets are for Block protection operation of MX30UF4G28AB. The block protection of MX30UF4G28AC use BP bits instead. Please refer to the individual datasheet for detailed specification.

Write Protection Comparison

The entire array of either part can be hardware write protected if the WP# pin is held low for greater than 100ns prior to the rising edge of WE#. For the MX30UF4G28AB, if the PT pin is high at power-on, the whole chip is protected, and the Block Protect command set is enabled. To unprotect, use the Block Unprotect commands 23h-24h + block address boundaries along with appropriate invert-bit setting and WP# pin high.

To re-protect all unprotected blocks, use the Block Protect (2Ah) command. To prevent any further changes in Block Protection status, issue "Solid Protect" command = 2Ch with PT pin high and WP# pin high (only way to unlock is after the next power cycle).

For the MX30UF4G28AC, if the PT pin is high at power-up, the entire chip comes up protected by volatile BP bits = 1. We can unprotect and re-protect portions of the array if WP# = 1 and using the "Set Feature" command EFh with Feature Address = A0h and BP bits data value. We can lock the BP bits by setting the "SP" Solid Protect Bit = 1, and the only way to unlock is the next power cycle. The SP bit can be set = 1, similar to setting the BP bits, using SetFeature command = EFh with feature address = A0h+data. To verify the sub-feature data is set correctly, we can Read the data value with GetFeature command EEh + Feature Address A0h (to read BP bit setting). We can check if block is protected or if SP bit is set by using "Block Protect Status Read" command = 7Ah + Block Address.

Please see the appropriate device datasheet for a more detailed description of Write Protect regions and command sequences.

Set Feature Operation (ONFI)

The feature address of the feature set operation is different. The MX30UF4G28AB uses 01h for timing mode setting, 80h for I/O drive strength configuration, and 81h for R/B# pull-down strength configuration, all of which are not supported by MX30UF4G28AC. The MX30UF4G28AC defines A0h for block protection operation which the MX30UF4G28AB does not. The differences are highlighted in Bold Italic type in the **Table 4-2**. Please refer to the Macronix datasheet for additional details.

Table 4-2: Definition of Feature Address

Feature description	Feature Address	
	MX30UF4G28AB	MX30UF4G28 AC
Timing Mode Setting	01h	N/A
Programmable I/O Drive Strength	80h	N/A
Programmable R/B# pull-down Strength	81h	N/A
Array Operation Mode	90h	90h
Block Protection Operation	N/A	A0h
Reserved	00h, 02-7Fh, 82h-8Fh, 91h-FFh	00h-8Fh, 91h-9Fh, A1h-FFh

5. Status Register Comparison

Status Register bit functions are the same (**Table 5-1**). Please refer to the Macronix datasheet for additional details.

Table 5-1. Status Register Comparison

Part Name	MX30UF4G28AB	MX30UF4G28AC
SR[0]	Page Read, Cache Read, Program/Cache program(page N)/ Erase	Page Read, Cache Read, Program/Cache program(page N)/ Erase
SR[1]	Cache Program (page N-1) Pass or Fail	Cache Program (page N-1) Pass or Fail
SR[2]	Not Used	Not Used
SR[3]	Not Used	Not Used
SR[4]	Not Used	Not Used
SR[5]	Ready/Busy for Internal Controller Program/Erase/Read Operation	Ready/Busy for Internal Controller Program/Erase/Read Operation
SR[6]	Ready/Busy	Ready/Busy
SR[7]	Write Protect	Write Protect

6. Package Pin Definition

The package physical dimension and pin definition of the MX30UF4G28AB and the MX30UF4G28AC is identical in 63-VFBGA.

However, the MX30UF4G28AB supports 48-TSOP and 63-VFBGA; whereas the MX30UF4G28AC only supports 63-VFBGA package type.

7. Device Identification

The 4th byte ID of MX30UF4G28AC is different from the MX30UF4G28AB. The difference is highlighted in Bold Italic type in the table (**Table 7-1 Device Identification**).

Table 7-1. Device Identification

Part Name		MX30UF4G28AB	MX30UF4G28AC
ID Code		C2h/AC ^h /90/15h/57h	C2h/AC ^h /90/ 11h /57h
ID Definition	1 st Byte	Manufacturer ID	Manufacturer ID
	2 nd Byte	Device ID	Device ID
	3 rd Byte	Number of Die per CE	Number of Die per CE
		Cell Structure	Cell Structure
		Number of Concurrently Programmed Pages	Number of Concurrently Programmed Pages
		Interleaved operations between Multiple die	Interleaved operations between Multiple die
		Cache program	Cache program
	4 th Byte	Page Size (2KB, bit1=0 & bit0=1)	Page Size (2KB, bit1=0 & bit0=1)
		Spare Area Size (28-byte per 512-byte), bit2=1	Spare Area Size (128-byte per page), bit2=0
		Sequential Read Cycle Time (bit7, bit3=1,0)	Sequential Read Cycle Time (bit7, bit3=1,0)
		Block Size (128KB excluding spare area, bit5=0 & bit4=1)	Block Size (128KB excluding spare area, bit5=0 & bit4=1)
		Organization	Organization
	5 th Byte	ECC level requirement,	ECC level requirement,
		Number of Planes per CE	Number of Planes per CE
		Plane Size	Plane Size
		Reserved	Reserved

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please contact Macronix.

Table 8-1. Datasheet Versions

Datasheet	Location	Date Issued	Revision
MX30UF4G28AB	Website	Feb. 2017	Rev. 1.1
MX30UF4G28AC	Website	Jan. 2019	Rev. 1.0

9. Summary

The Macronix MX30UF4G28AB and MX30UF4G28AC NAND flash share the same basic Read, Program, and Erase commands and have the same package dimension and pin-outs on 63-VFBGA. However, migrating to the MX30UF4G28AC may require firmware modifications to accommodate differences in spare area size. There are differences in the Write Protection implementation that will require firmware changes--if the feature is used.

10. Part Number Cross-Reference

Table 10-1. Part Number Cross Reference

Bus Width	Voltage	Package	Part Number	Part Number
x8	1.8V	48-TSOP	MX30UF4G28AB-TI	N/A
x8	1.8V	63-VFBGA	MX30UF4G28AB-XKI	MX30UF4G28AC-XKI

11. Revision History

Table 11-1. Revision History

Revision No.	Description	Page	Date
REV. 1	Initial Release	ALL	June 14, 2018
REV. 2	1. Removed Advanced Information page title to align product status.	ALL	December 27, 2019



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