The Comparison of Macronix Serial NOR Flash MX25L25645G/MX25L25673G with MX25L25635F

1. Introduction

This document highlights parameters which may require attention when comparing the MX25L25645G and MX25L25673G (55nm “G” Version) with the MX25L25635F (75nm “F” Version).

Generally, the G version is backward compatible with the F version as it is pin and command compatible with the basic Read/Program/Erase commands. There may be some differences if special features are used such as DTR mode, Advanced Sector Protection and Password protection.

The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information provided in this document is based on datasheets listed in Section *"10. Reference Documents"*. Newer versions of the datasheets may override the contents of this document. A comparison of key features is provided in *"Table 1-1: Key Feature Comparison"*.

Table 1-1: Key Feature Comparison

Feature		Part Number		
		MX25L25635F	**MX25L25645G**	**MX25L25673G**
Process Technology		75nm	55nm	55nm
VCC		2.7V – 3.6V	2.7V – 3.6V	2.7V – 3.6V
I/O		x1/x2/x4	x1/x2/x4	x1/x2/x4
Sector Size	4KB	V	V	V
	32KB	V	V	V
	64KB	V	V	V
Program Buffer Size		256Byte	256Byte	256Byte
Security OTP		4KBit	4KBit	4KBit
Read Interface	Normal Read	50MHz	50MHz	50MHz
	Fast Read 1x I/O	104MHz	120MHz	120MHz
	Fast Read 2x I/O	84MHz	80MHz (4 dummy cycles) 120MHz (8 dummy cycles)	80MHz (4 dummy cycles) 120MHz (8 dummy cycles)
	Fast Read 4x I/O	84MHz	80MHz (6 dummy cycles) 120MHz (8 dummy cycles)	80MHz (6 dummy cycles) 120MHz (8 dummy cycles)
Enhanced Frequency (x1/x2/x4)		133MHz	133MHz @ VCC=3.0V-3.6V	133MHz @ VCC=3.0V-3.6V
DTR (4x I/O)		NA	100MHz @ VCC=3.0V-3.6V	100MHz @ VCC=3.0V-3.6V
Features				
QPI Interface		Yes	Yes	Yes
Read Enhance Mode		Yes	Yes	Yes
Wrap around read mode		Yes	Yes	Yes
Configurable dummy cycle		Yes	Yes	Yes
Adjustable output driver		Yes	Yes	Yes
Suspend & Resume		Yes	Yes	Yes
Fast Boot (XIP) Mode		Yes	NA	NA
Quad Enable (QE)=1 fixed		NA	NA	Yes
BP Protection		Yes	Yes	Yes
Password protection		Yes	NA	NA
Volatile write protection		Yes	Yes	Yes
Non-volatile Write Protection		Yes	Yes	Yes
SFDP		JESD216	JESD216B	JESD216B
Factory Mode		NA	Support on -08G	Support on -08G

2. Package

MX25L25645G provides 8-SOP (200mil), 16-SOP (300mil) and 8-WSON (8x6mm)/(6x5mm) package options, which have pin out and physical dimensions identical to the MX25L25635F. MX25L25673G provides 8-SOP (200mil), 16-SOP (300mil) and 8-WSON (6x5mm) package options, except it does not have WP# pin and only the 16-SOP (300mil) package provides RESET# pin.

For more package information, please refer to the datasheets or contact our regional sales.

Table 2-1: Package Pins Comparison

16-PIN SOP (300mil)						
MX25L25673G	MX25L25645G	MX25L25635F		MX25L25635F	MX25L25645G	MX25L25673G
SIO3	NC/SIO3	DNU/SIO3	1 16	SCLK	SCLK	SCLK
VCC	VCC	VCC	2 15	SI/SIO0	SI/SIO0	SI/SIO0
RESET#	RESET#	RESET#	3 14	NC	NC	NC
NC	NC	NC	4 13	NC	NC	NC
NC	NC	NC	5 12	NC	NC	NC
NC	NC	NC	6 11	NC	NC	NC
CS#	CS#	CS#	7 10	GND	GND	GND
SO/SIO1	SO/SIO1	SO/SIO1	8 9	WP#/SIO2	WP#/SIO2	SIO2

8-WSON (8x6mm) / (6x5mm)						
MX25L25673G (6x5mm only)	MX25L25645G	MX25L25635F		MX25L25635F	MX25L25645G	MX25L25673G (6x5mm only)
CS#	CS#	CS#	1 8	VCC	VCC	VCC
SO/SIO1	SO/SIO1	SO/SIO1	2 7	RESET#/SIO3	RESET#/SIO3	SIO3
SIO2	WP#/SIO2	WP#/SIO2	3 6	SCLK	SCLK	SCLK
GND	GND	GND	4 5	SI/SIO0	SI/SIO0	SI/SIO0

8-PIN SOP (200mil)						
MX25L25673G	MX25L25645G	MX25L25635F		MX25L25635F	MX25L25645G	MX25L25673G
CS#	CS#	NA	1 8	NA	VCC	VCC
SO/SIO1	SO/SIO1		2 7		RESET#/SIO3	SIO3
SIO2	WP#/SIO2		3 6		SCLK	SCLK
GND	GND		4 5		SI/SIO0	SI/SIO0

3. Command Set

The core commands for read, erase, and program are unchanged between the F and G versions. For a full list of commands and a description of their functions, please refer to each product's datasheet.

Table 3-1: Command Set Comparison (Read/Erase/Program/ID Read)

Command	Symbol	Description	MX25L25635F	MX25L25645G MX25L25673G
Read	READ	Normal Read (1-1-1)	03h	03h
	FASTREAD	Fast Read (1-1-1)	0Bh	0Bh
	DREAD	Dual Output (1-1-2)	3Bh	3Bh
	2READ	2 I/O (1-2-2)	BBh	BBh
	QREAD	Quad Output (1-1-4)	6Bh	6Bh
	4READ	4 I/O (1-4-4)	EBh	EBh
	4DTRD	Quad I/O DT Read	-	EDh
Erase	SE	Sector Erase (4KB)	20h	20h
	BE32KB	Block Erase (32KB)	52h	52h
	BE	Block Erase (64KB)	D8h	D8h
	CE	Chip Erase	60h or C7h	60h or C7h
Program	PP	Page Program	02h	02h
	4PP	Quad Input Page Program	38h	38h
ID Read	RDID	Read ID	9Fh	9Fh
	RES	Read Electronic ID	ABh	ABh
	REMS	Read Electronic & Manufacturer ID	90h	90h
	QPIID	QPI ID Read	AFh	AFh

Table 3-1: Command Set Comparison (Register/Mode/Reset)

Command	Symbol	Description	MX25L25635F	MX25L25645G MX25L25673G
Register	RDSR	Read Status Register	05h	05h
	WRSR	Write Status Register	01h	01h
	RDSCUR	Read Security Register	2Bh	2Bh
	WRSCUR	Write Security Register	2Fh	2Fh
	RDFBR	Read Fast Boot Register	16h	16h
	WRFBR	Write Fast Boot Register	17h	17h
	ESFBR	Erase Fast Boot Register	18h	18h
Mode	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
	EQIO	Enable QPI	35h	35h
	RSTQIO	Disable QPI	F5h	F5h
	SBL	Set Burst Length	C0h	C0h
	PGM/ERS Suspend	Suspends Program/Erase	B0h	B0h
	PGM/ERS Resume	Resumes Program/Erase	30h	30h
	FMEN	Factory Mode Enable	-	41h (with -08G only)
Reset	NOP	No Operation	00h	00h
	RSTEN	Reset Enable	66h	66h
	RST	Reset Memory	99h	99h

Table 3-1: Command Set Comparison (Security)

Command	Symbol	Description	MX25L25635F	MX25L25645G MX25L25673G
Security	WRLR	Write Lock Register	2Ch	2Ch
	RDLR	Read Lock Register	2Dh	2Dh
	WRPASS	Write Password Register	28h	-
	RDPASS	Read Password Register	27h	-
	PASSULK	Password Unlock	29h	-
	WRSPB	SPB Bit Program	E3h	E3h
	ESSPB	All SPB Bit Erase	E4h	E4h
	RDSPB	Read SPB Status	E2h	E2h
	SPBLK	SPB Lock Set	A6h	-
	RDSPBLK	Read SPB Lock Register	A7h	-
	WRDPB	Write DPB Register	E1h	E1h
	RDDPB	Read DPB Register	E0h	E0h
	GBLK	Gang Block Lock	7Eh	7Eh
	GBULK	Gang Block Unlock	98h	98h

Table 3-1: Command Set Comparison (4-Byte Mode/EAR/4-Byte Command Set)

Command	Symbol	Description	MX25L25635F	MX25L25645G MX25L25673G
4-Byte Mode	EN4B	Enter 4-byte Address Mode	B7h	B7h
	EX4B	Exit 4-byte Address Mode	E9h	E9h
EAR	WREAR	Write Extended Address Register	C5h	C5h
	RDEAR	Read Extended Address Register	C8h	C8h
4-Byte Command Set	READ4B	Read Data Bytes Using 4 Bytes Address	13h	13h
	FASTREAD4B	Read Data Bytes at HigherSpeed using 4 Bytes Address	0Ch	0Ch
	DREAD4B	Dual Output Fast Read Using 4 Byte Address	3Ch	3Ch
	2READ4B	Dual Input/Output Fast Read Using 4 Byte Address	BCh	BCh
	QREAD4B	Quad Output Fast Read Using 4 Byte Address	6Ch	6Ch
	4READ4B	Quad Input/Output Fast Read Using 4 Byte Address	ECh	ECh
	SE4B	Sector Erase Using 4 Byte Address	21h	21h
	BE32K4B	Block Erase 32KB Using 4 Byte Address	5Ch	5Ch
	BE4B	Block Erase 64KB Using 4 Byte Address	DCh	DCh
	PP4B	Page Program Using 4 Byte Address	12h	12h
	4PP4B	Quad Page Program Using 4 Byte Address	3Eh	3Eh

4. Data Protection

Both F and G version products provide two write protection modes to easily protect sectors from inadvertent changes and will be discussed in more details below.

4-1. BP bit Block Protection

Both Macronix MX25L25635F and MX25L25645G/MX25L25673G can use BP bits in the Status Register to select groups of memory areas for write protection. All the regions protected by F version can be protected by G version with the identical BP setting. Please refer to the following comparison table.

Table 4-1: Block Protection (BP) Comparison of MX25L25635F and MX25L25645G/MX25L25673G

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level	
BP3	BP2	BP1	BP0	MX25L25635F	MX25L25645G MX25L25673G
0	0	0	0	0 (none)	0 (none)
0	0	0	1	1 (1 block, protected block 511th)	1 (1 block, protected block 511th)
0	0	1	0	2 (2 blocks, protected block 510th-511th)	2 (2 blocks, protected block 510th-511th)
0	0	1	1	3 (4 blocks, protected block 508th-511th)	3 (4 blocks, protected block 508th-511th)
0	1	0	0	4 (8 blocks, protected block 504th-511th)	4 (8 blocks, protected block 504th-511th)
0	1	0	1	5 (16 blocks, protected block 496th-511th)	5 (16 blocks, protected block 496th-511th)
0	1	1	0	6 (32 blocks, protected block 480th-511th)	6 (32 blocks, protected block 480th-511th)
0	1	1	1	7 (64 blocks, protected block 448th-511th)	7 (64 blocks, protected block 448th-511th)
1	0	0	0	8 (128 blocks, protected block 384th-511th)	8 (128 blocks, protected block 384th-511th)
1	0	0	1	9 (256 blocks, protected block 256th-511th)	9 (256 blocks, protected block 256th-511th)
1	0	1	0	10 (512 blocks, protected all)	10 (512 blocks, protected all)
1	0	1	1	11 (512 blocks, protected all)	11 (512 blocks, protected all)
1	1	0	0	12 (512 blocks, protected all)	12 (512 blocks, protected all)
1	1	0	1	13 (512 blocks, protected all)	13 (512 blocks, protected all)
1	1	1	0	14 (512 blocks, protected all)	14 (512 blocks, protected all)
1	1	1	1	15 (512 blocks, protected all)	15 (512 blocks, protected all)

4-2. Individual Sector Protection Mode

The second mode uses an Individual Sector Protection method.

Both Macronix MX25L25635F and MX25L25645G/MX25L25673G have the ability to protect individual 4KB and 64KB sectors and blocks of memory. Individual block protection is only effective after executing the WPSEL command. This one-time-use command permanently disables the block group protection method (Status Register BP bits) and activates individual block protection. The WPSEL command is common to both F and G versions.

4-2-1. Lock Register

Operating individual sector protection feature on G version is similar with F version. Both F and G version have SPB and DPB to implement individual sector protection feature.

To enhance the security of the protection feature, MX25L25645G/MX25L25673G provides SPB Lock Down feature. Once SPBLKDN(Bit 6) is set, SPB bit value can not be changed again and it is read-only.

The Lock Register has slight difference, please check the comparison table (*"Table 4-2: Lock register Comparison"*) and refer to MX25L25645G/MX25L25673G datasheets for more detailed information.

Table 4-2: Lock register Comparison

	MX25L25635F	MX25L25645G MX25L25673G
bit 0	Reserved	RFU
bit 1	Solid Protection Mode Lock Bit	RFU
bit 2	Password Protection Mode Lock Bit	RFU
bit 3	Reserved	RFU
bit 4	Reserved	RFU
bit 5	Reserved	RFU
bit 6	Reserved	SPBLKDN
bit 7-15	Reserved	RFU

5. Register Comparison

The MX25L25645G Status Register bits are backward compatible with the registers of the MX25L25635F. For MX25L25673G, the Quad Enable (QE) bit is permanently set to "1" and does not have SRWD bit.

Table 5-1: Status Register Comparison

	MX25L25635F	MX25L25645G	MX25L25673G
bit 0	WIP (write in progress bit)	WIP (write in progress bit)	WIP (write in progress bit)
bit 1	WEL (write enable latch)	WEL (write enable latch)	WEL (write enable latch)
bit 2	BP0 (level of protected block)	BP0 (level of protected block)	BP0 (level of protected block)
bit 3	BP1 (level of protected block)	BP1 (level of protected block)	BP1 (level of protected block)
bit 4	BP2 (level of protected block)	BP2 (level of protected block)	BP2 (level of protected block)
bit 5	BP3 (level of protected block)	BP3 (level of protected block)	BP3 (level of protected block)
bit 6	QE (Quad Enable)	QE (Quad Enable)	QE (Quad Enable) permanently enabled.
bit 7	SRWD (status register write protect)	SRWD (status register write protect)	Reserved

Basically, Configuration Register bits on G version are backward compatible with the registers of F version Please note that the ODS setting is slightly different between G and F version. G version has added Bit4 for Preamble bit Enable to improve data capture reliability while the flash memory is running in high frequency.

Table 5-2: Configuration Register Comparison

	MX25L25635F	MX25L25645G MX25L25673G
bit 0	ODS 0 (output driver strength)	ODS 0 (output driver strength)
bit 1	ODS 1 (output driver strength)	ODS 1 (output driver strength)
bit 2	ODS 2 (output driver strength)	Reserved
bit 3	TB (top/bottom selected)	TB (top/bottom selected)
bit 4	Reserved	PBE (Preamble bit Enable)
bit 5	4 BYTE	4 BYTE
bit 6	DC0 (Dummy cycle 0)	DC0 (Dummy cycle 0)
bit 7	DC1 (Dummy cycle 1)	DC1 (Dummy cycle 1)

The MX25L25645G/MX25L25673G Security Register bits are backward compatible with the registers of the MX25L25635F.

Table 5-3: Security Register Comparison

	MX25L25635F	MX25L25645G MX25L25673G
bit 0	Secured OTP indicator bit	Secured OTP indicator bit
bit 1	LDSO (indicate if lock-down)	LDSO (indicate if lock-down)
bit 2	PSB (Program Suspend bit)	PSB (Program Suspend bit)
bit 3	ESB (Erase Suspend bit)	ESB (Erase Suspend bit)
bit 4	Reserved	Reserved
bit 5	P_FAIL	P_FAIL
bit 6	E_FAIL	E_FAIL
bit 7	WPSEL	WPSEL

6. Electrical Characteristics

The comparison of DC and AC characteristics are shown in Tables 6-1 and 6-2:

Table 6-1: DC Characteristics

DC Performance		MX25L25635F	MX25L25645G MX25L25673G
Active Current	Read (4I/O)	25mA @133MHz	25mA @133MHz 20mA @104MHz
	Erase	25mA	25mA
	Program	20mA	25mA
VCC Standby Current		50uA	100uA
Deep Power Down Current		20uA	20uA

(Note: All of the data shown in Table 6-1 are maximum values).

Table 6-2: AC Characteristics

AC Performance			MX25L25635F	MX25L25645G MX25L25673G
Erase Time	4KB	typ	30ms	30ms
		max	120ms	400ms
	32KB	typ	150ms	180ms
		max	650ms	1000ms
	64KB	typ	280ms	380ms
		max	650ms	2000ms
	Chip Erase	typ	110s	110s
		max	150s	150s
Program Time	Byte	typ	16us	15us
		max	30us	30us
	Page (256-Byte)	typ	0.5ms	0.25ms
		max	1.5ms	0.75ms
	Write Status Register	typ	-	-
		max	40ms	40ms
Erase/Program Cycles		typ	100,000	100,000
tCLQV (4I/O)	15pf	max	6ns	6ns
	30pf	max	8ns	8ns

7. Memory Organization

The memory and sector architecture of the MX25L25645G/MX25L25673G flash memory are identical to the MX25L25635F flash memory.

8. Device Identification

The Manufacturer ID and Device ID values of the G version flash memory are identical to the F version flash memory.

Table 8-1: Manufacturer ID & Device ID

ID item		MX25L25635F	MX25L25645G MX25L25673G
RDID	Manufacturer ID	C2h	C2h
	Type	20h	20h
	Density	19h	19h
RES	Electronic ID	18h	18h
REMS	Manufacturer ID	C2h	C2h
	Device ID	18h	18h
QPIID	Manufacturer ID	C2h	C2h
	Type	20h	20h
	Density	19h	19h

9. Summary

Generally, the MX25L25645G is backward compatible with the MX25L25635F as it is pin and command compatible with the basic Read/Program/Erase commands, while MX25L25673G does not have WP# pin and has RESET# in 16-SOP (300mil) package only.
There may be some differences if special features are used such as DTR mode, Advanced Sector Protection and Password protection, or MX25L25673G is default as Quad I/O enable (QE bit=1).

10. Reference Documents

Table 10-1 shows the datasheet versions used for comparison in this application note. For the most current Macronix specification, please refer to the Macronix Website at http://www.macronix.com

Table 10-1: Datasheet Version

Datasheet	Location	Date Issued	Versions
MX25L25635F	Macronix Website	September 26, 2016	Rev. 1.5
MX25L25645G	Macronix Website	November 25, 2022	Rev 2.0
MX25L25673G	Macronix Website	May 29, 2025	Rev 1.9

11. Revision History

Table 11-1: Revision History

Revision No.	Description	Page	Date
Rev. 1	Initial Release	ALL	February 13, 2017
Rev. 2	Added MX25L25673G	ALL	June 12, 2017
Rev. 3	1. Added "Macronix Proprietary" footnote; 2. Revised the content of Table 1-1; 3. Updated Table 10-1.	ALL	November 14, 2019
Rev. 4	1. Modified the title; 2. Revised the content of Table 3-1; 3. Updated Table 10-1.	P1, 4, 6-7	June 25, 2025

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