1.8V MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY MCP WITH MULTIPLEXED, BURST MODE, PSEUDO SRAM

MX65U28F64

MX65U64F32

DATASHEET

128M-BIT/64M-BIT [x 1/x 2/x 4] 1.8V CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY MCP

SERIAL FLASH

FEATURES

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 128Mb/64Mb MXSMIO® Serial Flash
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.0V to 1.4V
- High Performance
  - Fast read for SPI mode
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 84MHz with 4 dummy cycles, equivalent to 168MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast read for QPI mode
    - 4 I/O: 84MHz with 2+2 dummy cycles, equivalent to 336MHz
    - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast program time: 1.2ms/3ms (typ./max.)/page (256-byte per page)
  - Byte program time: 12us (typ.)
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
  - Fast erase time: 60ms (typ.)/sector (4K-byte per sector); 250ms(typ.)/block (32K-byte per block), 500ms(typ.)/block (64K-byte per block); 50s/chip (typ.) (64Mb)/72s/chip (typ.) (128Mb)
- Low Power Consumption
  - Low active read current: 20mA(typ.) at 104MHz, 15mA(typ.) at 84MHz
  - Low active erase/programming current: 20mA (typ.)
  - Standby current: 30uA (typ.)
- Deep Power Down: 5uA(typ.)
- Typical 100,000 erase/program cycles
- 10 years data retention
- Operating Temperature Range
  - Wireless Grade: -25°C~85°C
- Package
  - MCP BGA: 0.5mm ball pitch
  - 6.2x7.7mm, 56 ball

PSEUDO SRAM

FEATURES

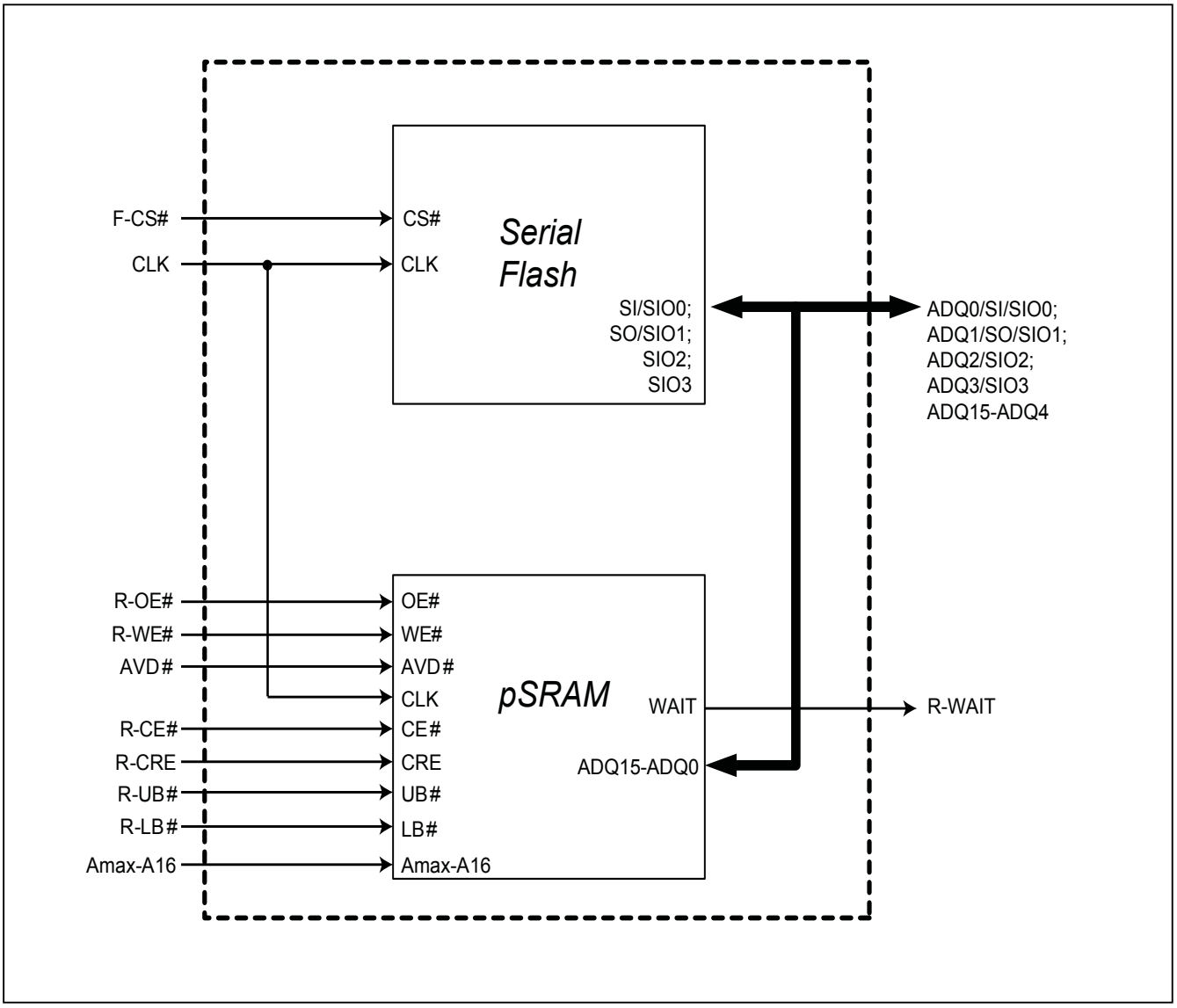
- Single device supports asynchronous and burst operation
- Mixed Mode supports asynchronous write and synchronous read operation
- Dual voltage rails for optional performance
  - VDD: 1.7V~1.95V
  - VDDQ: 1.7V~1.95V
- Multiplexed address and data bus
  - ADQ0~ADQ15
- Asynchronous mode read access : 70ns
- Burst mode for Read and Write operation
  - 4, 8, 16 Words (or 8,16,32 Bytes) or Continuous
- Low Power Consumption
  - Asynchronous Operation < 25mA
  - Burst operation < 45mA (@133MHz)
  - Standby < 250uA (max.)
- Low Power Feature
  - Reduced Array Refresh
  - Temperature Controlled Refresh
- Operation Frequency up to 133MHz
- Operating Temperature Range
  - Wireless Grade: -25°C~85°C

Product Selection Guide

Device	Density		Speed		Package Type
	Flash	pSRAM	Flash	pSRAM	
MX65U64F32MXJW	64Mb	32Mb	104MHz	133MHz	6.2x7.7 56-TFBGA
MX65U28F64MXJW *	128Mb	64Mb	104MHz	133MHz	6.2x7.7 56-TFBGA

* Advanced Information

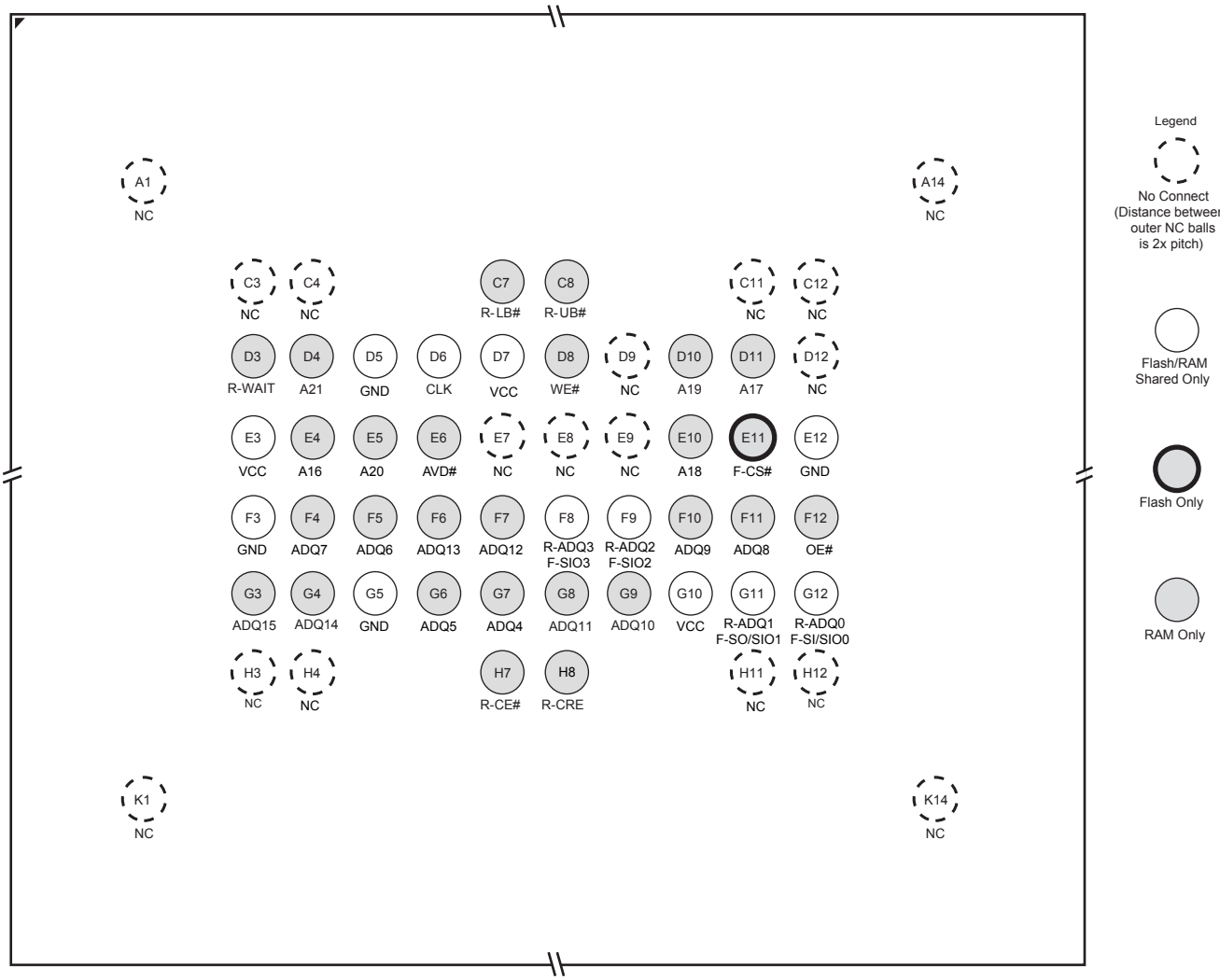
BLOCK DIAGRAM



PIN CONFIGURATIONS

pSRAM Based Pinout, 56-Ball, TFBGA

(Top View, Balls Facing Down)



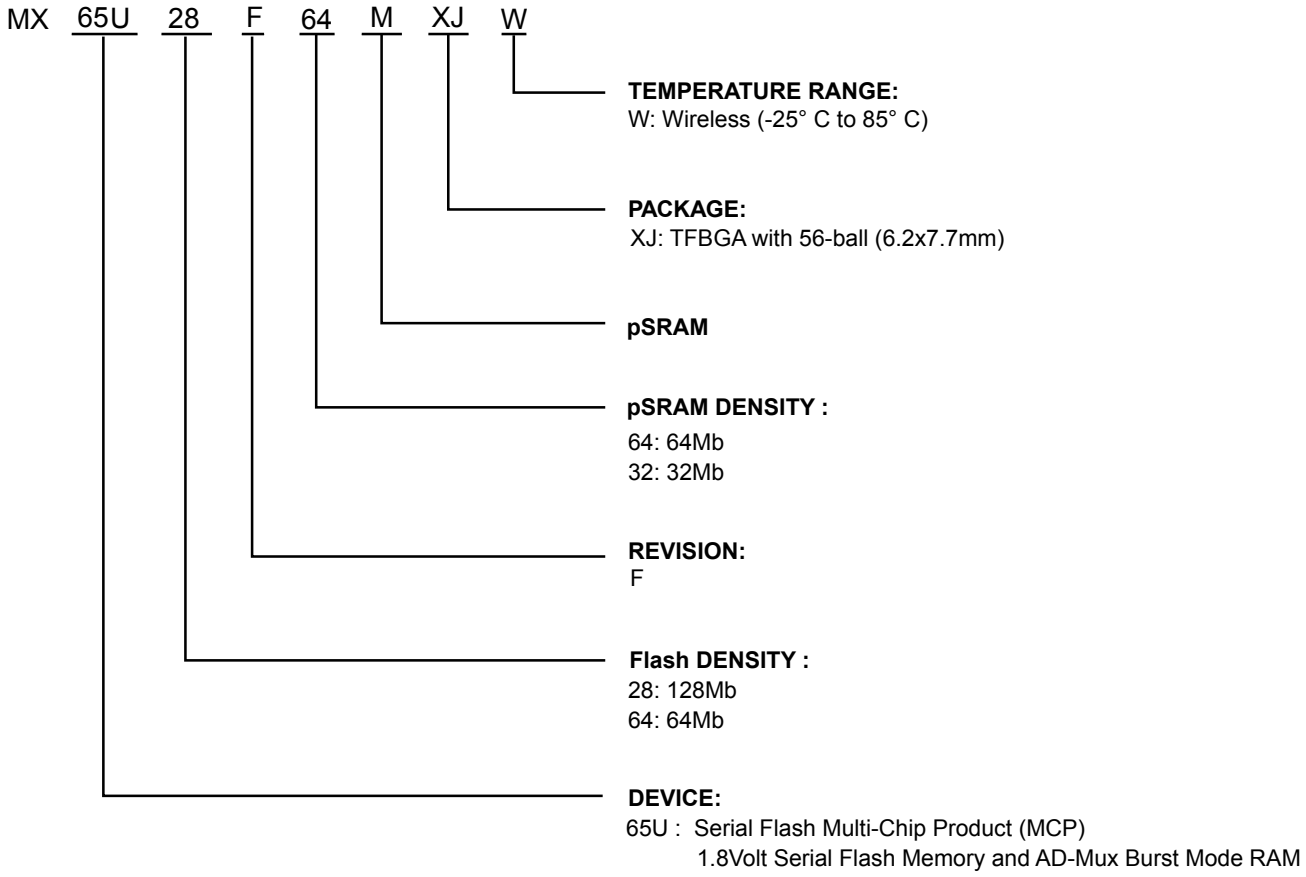
Notes

1. A0~A3 Addresses are shared between Flash and RAM.
2. A21 is only for 64Mb pSRAM. For MX65U64F32 product, please keep A21 as "1" during operation.

PIN DESCRIPTION

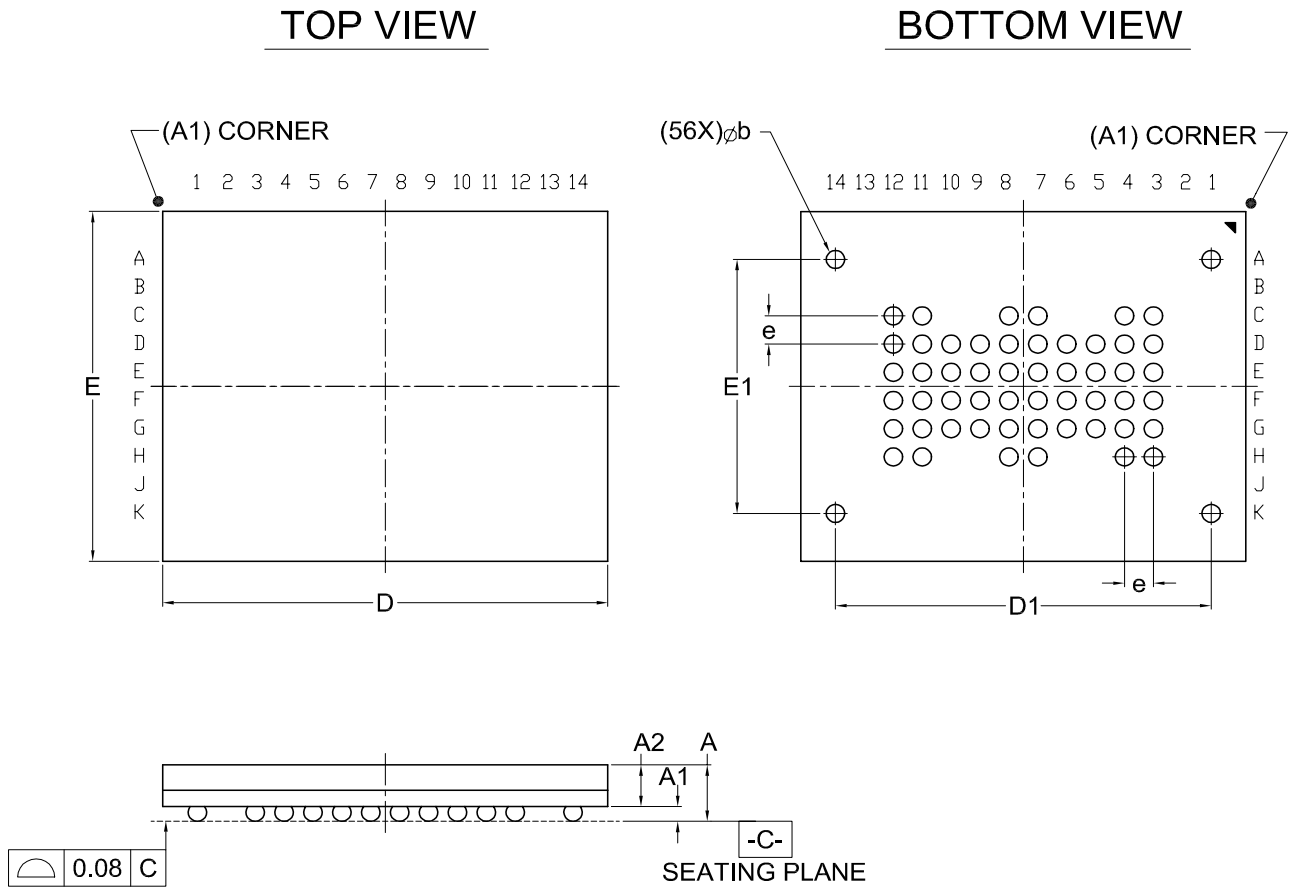
SYMBOL	DESCRIPTION	Flash	RAM
Amax-A16	Address Inputs		V
SI/O ; ADQ15~ADQ0	Multiplexed Data Inputs/Outputs	V	V
OE#	Output Enable Input		V
WE#	Write Enable Input		V
VCC	Device Power Supply (1.70V~1.95V)	V	V
GND	Device Ground	V	V
NC	No Connection	V	V
RDY	Ready output, the status of the Burst Read	V	V
WAIT	Wait		V
CLK	Clock	V	V
AVD#	Address Valid Data input.		V
R-CE#	Chip-enable input for pSRAM.		V
F-CS#	Chip-select input for Flash.	V	
R-CRE	Control Register Enable (pSRAM).		V
R-UB#	Upper Byte Control (pSRAM).		V
R-LB#	Lower Byte Control (pSRAM).		V

PART NAME DESCRIPTION



PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 56BALL(7.7X6.2X1.2MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	---	---
	Nom.	---	0.21	---	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.20	0.26	---	0.35	7.8	---	6.3	---	---
Inch	Min.	---	0.006	0.026	0.010	0.299	---	0.240	---	---
	Nom.	---	0.008	---	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.047	0.010	---	0.014	0.307	---	0.248	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4264	1				

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Modified Fast program time & Byte program time	P2	MAY/10/2012
1.0	1. Removed "Advanced Information"	P1,2	JUL/22/2013
	2. Modified chip erase time: 50s(typ.) (64Mb)/72s(typ.) (128Mb)	P2	
	3. Removed MX65U64E32EXJW	P3	
1.1	1. Modified BLOCK DIAGRAM and PIN CONFIGURATIONS	P4,5	JUL/30/2014
	2. Removed MX65U64F32EXJW and MX65U28F64EXJW	P3,7	
	3. Added MX65U64F32MXJW, and MX65U28F64MXJW as Advanced Information	P3,7	

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